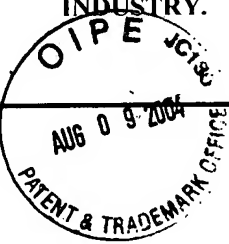


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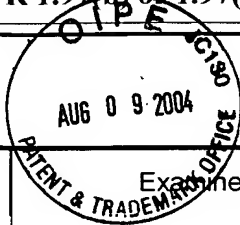
TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT (Under 37 CFR 1.97(b) or 1.97(c))				Docket No. BUR920040086US1	
In Re Application Of: Rankin et al.					
Application No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.
10/710602	07/23/04	Unassigned	024241		
Title: METHOD TO SELECTIVELY CORRECT CRITICAL DIMENSION ERRORS IN THE SEMICONDUCTOR					
INDUSTRY.					
					
Address to: Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450					
37 CFR 1.97(b)					
1. <input checked="" type="checkbox"/> The Information Disclosure Statement submitted herewith is being filed within three months of the filing of a national application other than a continued prosecution application under 37 CFR 1.53(d); within three months of the date of entry of the national stage as set forth in 37 CFR 1.491 in an international application; before the mailing of a first Office Action on the merits, or before the mailing of a first Office Action after the filing of a request for continued examination under 37 CFR 1.114.					
37 CFR 1.97(c)					
2. <input type="checkbox"/> The Information Disclosure Statement submitted herewith is being filed after the period specified in 37 CFR 1.97(b), provided that the Information Disclosure Statement is filed before the mailing date of a Final Action under 37 CFR 1.113, a Notice of Allowance under 37 CFR 1.311, or an Action that otherwise closes prosecution in the application, and is accompanied by one of:					
<input type="checkbox"/> the statement specified in 37 CFR 1.97(e);					
OR					
<input type="checkbox"/> the fee set forth in 37 CFR 1.17(p).					

TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT

(Under 37 CFR 1.97(b) or 1.97(c))

Docket No.
BUR920040086US1

In Re Application: Rankin et al.



Application No.

Filing Date

Examiner

Customer No.

Group Art Unit

Confirmation No.

10/710602

07/23/04

Unassigned

024241

**METHOD TO SELECTIVELY CORRECT CRITICAL DIMENSION ERRORS IN THE
INDUSTRY.****Payment of Fee**

(Only complete if Applicant elects to pay the fee set forth in 37 CFR 1.17(p))

- ☐ A check in the amount of _____ is attached.
- ☒ The Director is hereby authorized to charge and credit Deposit Account No. **09-0456**
as described below.
- ☒ Charge the amount of _____
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***This certificate may only be used if paying by deposit account.**

Signature

Dated: **Aug. 5, 2004**

William D. Sabo, Esq.

Reg. No.: 27,465

IP Law Department

IBM Microelectronics

1000 River Street - 972E

Essex Junction, VT 05452

Tel. No.: 802-769-9454

CC:



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
PATENT APPLICATION

Applicant: Rankin et al. Serial No.: 10/710602
Filed: 07/23/2004 Atty. Docket: BUR920040086US1
Title: METHOD TO SELECTIVELY CORRECT CRITICAL DIMENSION ERRORS
IN THE SEMICONDUCTOR INDUSTRY.

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR 1.56, 1.97, 1.98

Honorable Commissioner of Patents and Trademarks
Washington, D. C. 20231

Sir:

Applicants submit herewith form PTO-1449, listing patents, publications, or other information of which they are aware which they believe may be material to patentability pursuant to 37 CFR 1.56(b), and in respect of which there may be a duty to disclose under 37 CFR 1.56(a), together with legible copies of the patents, publications, or other information listed.

While the items submitted with this Information Disclosure Statement may be material to patentability pursuant to 37 CFR 1.56, in accordance with 37 CFR 1.97(h) it shall not be construed to be an admission that any patent, publication, or other information cited is "prior art" or is material to patentability for this invention unless specifically designated as such. In accordance with 37 CFR 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other information material to patentability, as defined in 37 CFR 1.56(b), exists.

Respectfully submitted,

Date: Aug. 5, 2004

By:

William D. Sabo, Esq.
Registration No. 27,465
Attorney for Applicants
IBM Corporation
Intellectual Property Law - Mail Stop 972E
1000 River Street
Essex Junction, Vermont 05452

INFORMATION DISCLOSURE CITATION <i>(Use several sheets if necessary)</i>				Docket Number (Optional) BUR920040086US1		Application Number 10/710602	
				Applicant(s) Rankin et al.			
				Filing Date 07/23/04		Group Art Unit	

U.S. PATENT DOCUMENTS							
*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

U.S. PATENT APPLICATION PUBLICATIONS							
*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS								
	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO

OTHER DOCUMENTS		<i>(Including Author, Title, Date, Pertinent Pages, Etc.)</i>
		Chung et al., DEEP-SUBMICROMETER MOS DEVICE FABRICATION USING A PHOTORESIST-ASHING TECHNIQUE, IEEE Electron Device Letters, Vol. 9, No. 4, April 1988, pages 186-188.
		Chiong et al., CONTRAST ENHANCEMENT OF RESIST IMAGES BY SURFACE CROSSLINKAGE, IBM Technical Disclosure Bulletin, Vol. 31, No. 3, August 1988, page 349.

EXAMINER	DATE CONSIDERED
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EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.